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Tracking-parallel analog-to-digital converter

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Abstract. Amid the rapid evolution of digital signal processing systems, the development of new analog-to-digital converter architectures capable of ensuring high dynamic accuracy without an excessive increase in component count has become a priority. The aim of the work was to improve the dynamic accuracy and speed of the analog-to-digital conversion process by developing and investigating an improved tracking-parallel architecture. Methods of automatic control theory, circuit analysis of pulse devices, and mathematical modelling of quantisation errors were applied to achieve the set tasks. The article detailed the operating principle of the proposed device, which is based on the synergy of an inertial tracking loop and a high-speed parallel residue converter. It was proven that introducing a dynamic error measurement stage allows compensating for the output code lag relative to the input signal, typical for traditional tracking systems, thereby eliminating slope overload distortion. The dependence of the input signal dynamic range expansion on the resolution of the parallel block was analytically substantiated, allowing for flexible system adaptation to specific application requirements. Comparative analysis results indicated that the proposed structure provides a significant gain in hardware complexity, enabling high resolution using orders of magnitude fewer precision comparators compared to counterparts. Furthermore, critical requirements for the speed of the operational amplifier and the digital-to-analog converter in the feedback loop were defined to ensure stable operation across the entire frequency range. The practical value of the research lies in developing recommendations for designing competitive integrated circuits oriented towards use in portable devices, medical equipment, and industrial automation systems

Keywords: hybrid architecture; slope overload; dynamic error compensation; residue signal; signal slew rate; hardware efficiency; high-precision

INTRODUCTION

The modern stage of scientific and technological progress is dominated by comprehensive digitalisation, which is permeating all areas of human activity, from ultra-fast 5G and 6G telecommunications networks to precision biomedical implants and autonomous vehicle control systems. A key element of any information

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and measurement system that provides interaction between the analogue physical environment and digital computing resources is an analogue-to-digital converter. The requirements for these devices are growing exponentially: modern applications require not only high sampling frequencies for processing broadband signals, but also high bit depths to ensure the necessary dynamic range, all while facing strict limitations on power consumption and chip area.

The problem becomes particularly acute in the context of the development of the concept of edge computing and compute-in-memory architectures. S. Xiao *et al*. (2025) noted in their in-depth review that the efficiency of analogue-to-digital converters is becoming a critical factor (a "bottleneck") that determines the overall performance of artificial intelligence systems, since a significant portion of energy is spent on converting data before it is processed. However, the design of analogue-to-digital converters traditionally faces a fundamental technological compromise: increasing speed and accuracy inevitably leads to a disproportionate increase in hardware complexity. This necessitates the search for new, non-traditional architectural solutions that can circumvent the limitations of classical conversion methods. The scientific community and leading microelectronics developers are actively working on the creation of hybrid architectures, trying to combine the advantages of different conversion methods. The ultra-high-speed segment is dominated by parallel analogue-to-digital converters (Flash ADCs). However, as K. Krishna & N. Nambath (2024) highlighted, this approach faces the problem of "tyranny of numbers": N-bit conversion requires 2^{N-1} comparators. The study emphasised that with an increase in bit width above 8 bits, the exponential growth in input capacity and power consumption makes Flash architecture economically and technically inefficient for modern portable devices.

To solve this problem, multi-stage schemes are being developed. D.-R. Oh *et al*. (2022) proposed a two-step Flash architecture that uses the Sample-and-Hold Sharing technique. The study demonstrated that this approach significantly reduces chip area and power consumption compared to a full Flash analogue-to-digital converter. However, analysis of their study demonstrated that two-step circuits introduce additional delay (latency) and impose high requirements on the accuracy of interstage amplifiers and timing diagram matching, which complicates their calibration. Another promising direction is the development of Successive Approximation Register Analogue-to-Digital Converters (SAR ADCs). K.E. Lozada *et al*. (2024) examined SAR-assisted hybrid analogue-to-digital converters, where the SAR block is used for accurate but energy-efficient determination of the least significant bits. The study argued that such hybrids are optimal for medium-speed applications. However, a fundamental limitation remains the iterative nature of the successive approximation algorithm, which requires several clock cycles to obtain a single reading, limiting its application in real-time systems with ultra-fast signal changes.

Research into oversampling methods occupies a separate niche. A. Verreault *et al*. (2024) conducted a detailed analysis of current trends in this field, highlighting the effectiveness of delta-sigma modulators for achieving high resolution. However, as the study noted, these methods are effective mainly for narrowband signals, and expanding the passband requires a disproportionate increase in clock frequency, which again runs into energy limitations. There is growing interest in asynchronous and tracking architectures, in particular, level-crossing analogue-to-digital converters (Level-Crossing ADC), which generate data only at moments of change in the input signal. F. Shahbazi & H. Shamsi (2025) demonstrated the promise of such systems for biomedical applications (electrocardiography, electroencephalography), where signals are sparse in time. This achieves low power consumption during periods of low signal activity. This idea was confirmed by M. Timmermans *et al*. (2024), presenting the implementation of a Continuous-Time Level Crossing analogue-to-digital converter with dynamic comparator offset, demonstrating record energy efficiency. Developing the idea of hybridisation, H. Tang *et al*. (2024) proposed a combined Level-Crossing Successive-Approximation-Register (LC-SAR) architecture that attempts to combine the adaptability of tracking systems with the accuracy of SAR.

Despite significant achievements, classic tracking systems (Tracking ADC) have a critical drawback that limits their widespread use: limited slew rate. The system can process signal changes in only one quantisation step per clock cycle. If the input signal changes faster, a dynamic slope overload error occurs, leading to information loss. O.D. Azarov *et al*. (2020) investigated methods for improving the performance of tracking analogue-to-digital converters by introducing weight redundancy into the feedback structure. This improved the convergence of transient processes, but it was not possible to eliminate the problem of lag during sharp signal jumps without changing the very philosophy of the converter design. Thus, there is a pressing scientific and technical problem: how to ensure the high accuracy and energy efficiency inherent in tracking systems, while guaranteeing the instantaneous response to rapid signal changes characteristic of Flash analogue-to-digital converters, without increasing the hardware complexity to unacceptable limits.

The study aimed to improve the dynamic accuracy and expand the frequency range of data converters by studying the innovative principle of a tracking-parallel analogue-to-digital converter, protected by Patent No. 158494 (2025). The main objective of the study was to achieve a synergistic combination of an inertial tracking circuit (for processing low-frequency components) and a non-inertial parallel analogue-to-digital converter with low bit depth (for measuring and

compensating for fast dynamic errors) that would overcome the limitations of both basic architectures. To achieve this goal, it was necessary to solve the following tasks: to perform a structural and functional analysis of the architecture proposed in the patent and describe the mechanism of interaction between the tracking and parallel channels; to develop a mathematical model of the converter that describes the processes of error signal formation and its compensation in dynamic mode; determine the analytical conditions under which the slope overload effect is eliminated, and establish the dependence of the maximum speed on the bit width of the auxiliary Flash-analogue-digital converter, conducting a comparative assessment of the technical and economic indicators (hardware complexity, energy consumption) of the developed solution in comparison with traditional Flash and SAR analogues.

MATERIALS AND METHODS

Subject of research: tracking-parallel architecture. Based on an analysis of the shortcomings of existing systems, the study proposed a tracking-parallel analogue-to-digital converter, protected by Patent No. 158494 (2025). This architecture, shown in Figure 1, combines the advantages of tracking and parallel conversion methods.

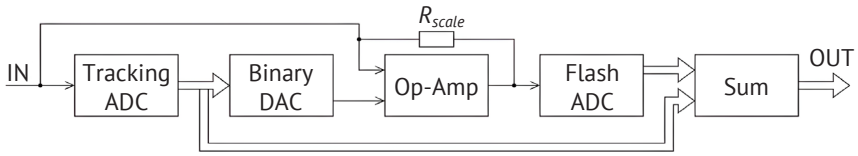

Figure 1. Block diagram of a tracking-parallel analogue-to-digital converter

Notes: IN – input bus; Binary DAC – binary digital-to-analogue converter; R_{scale} – scale resistor; Op-Amp – operational amplifier; Flash ADC – parallel analogue-to-digital converter; Sum – adder; OUT – output bus

Source: Patent No. 158494 (2025)

The device consists of the following main functional units: a tracking analogue-to-digital converter, a binary digital-to-analogue converter, an operational amplifier, a parallel analogue-to-digital converter (Flash analogue-to-digital converter), an adder and an input analogue signal. The tracking analogue-to-digital converter is a basic circuit containing a reversible counter and a comparator. It is designed to track the main (low-frequency) component of the input signal. A binary digital-to-analogue converter is a digital-to-analogue converter included in the feedback circuit of a tracking analogue-to-digital converter. It generates a voltage corresponding to the current counter code. An operational amplifier with a scaling resistor performs the function of analogue subtraction and scaling. It extracts the difference between the input signal and the feedback signal. A parallel analogue-to-digital converter (Flash analogue-to-digital converter) is an auxiliary high-speed analogue-to-digital converter with a small number of bits that digitises the error signal (residual). The adder is a digital node that combines the codes of the tracking analogue-to-digital converter and the Flash analogue-to-digital converter to obtain the result. The input analogue signal is the signal to be converted.

The device contains an input bus of a tracking analogue-to-digital converter, which is connected to the first input of the operational amplifier, as well as to a scale resistor. the information output of the tracking analogue-to-digital converter is connected to a binary digital-to-analogue converter, as well as to the second input of the adder, the output bus of the binary digital-to-analogue converter is connected to an operational amplifier, the output of the operational amplifier is connected to the input bus of the parallel analogue-to-digital converter, as well as to the scale resistor, the information output of the parallel analogue-to-digital converter is connected to the first input of the adder, the device also contains an output bus. The input signal is applied to the input bus of the tracking analogue-to-digital converter, from where a binary code is immediately obtained, which is then fed to a binary digital-to-analogue converter to reproduce the part of the input signal that was successfully converted by the tracking analogue-to-digital converter. This part of the signal similarly enters an operational amplifier, which amplifies the difference between the two signals on a certain scale using a scaling resistor. At the same time, the input signal that enters one of the inputs of this amplifier is subtracted from the signal that was balanced by the tracking analogue-to-digital converter. The difference between them represents the error at a given clock cycle, since the tracking analogue-to-digital converter always has some error, especially with rapid signal changes. This error may persist if the input signal changes rapidly. If it is stable, the error is minimised after a few cycles when the tracking analogue-to-digital converter catches up with the input signal. This is accelerated by the inability of the tracking analogue-to-digital converter to calculate the difference, which is transferred to a parallel analogue-to-digital converter (not multi-bit) that adds this difference.

A binary digital-to-analogue converter is used to determine the part of the signal that the tracking analogue-to-digital converter was able to convert. If the parallel analogue-to-digital converter successfully compensated for the difference remaining from the tracking analogue-to-digital converter, the correct value will be obtained on the first clock cycle. If this is

not possible, the device will operate for several cycles until the output code fully corresponds to the input analogue signal. However, this number of cycles is much smaller than in a simple tracking analogue-to-digital converter, thanks to the introduction of a parallel analogue-to-digital converter 6, which constantly monitors this difference and, if possible, compensates for it, obtaining the code on the first cycle, corresponding to the signal value. The operational amplifier (difference amplifier) is connected according to the differential amplifier circuit. It calculates and amplifies the difference between the analogue signals at its inputs (i.e. it extracts the unbalanced value of the analogue signal). The operational amplifier is used with a scale resistor, which is selected once to restore the range of the next analogue-to-digital converter, i.e. it sets the gain of the difference between the input signals. At the output, the device contains an adder (or other computing device) that combines two codes received from the tracking and parallel analogue-to-digital converters, respectively, and forms an output code that is sent to the output bus.

The device operates based on task parallelisation. The tracking circuit continuously attempts to equalise its output voltage with the input signal by incrementing or decrementing the counter (pulling the code). At moments of rapid changes in the input signal, when the tracking circuit cannot keep up (a dynamic error occurs), a voltage proportional to the magnitude of this lag is formed at the output of the operational amplifier. A parallel analogue-to-digital converter instantly measures this discrepancy voltage. The adder instantly adds the measured error to the current counter value. Thus, even if the counter "lags behind", the total code at the output of the device corresponds to the actual value of the input signal. This eliminates the slope overload effect without the need to increase the clock frequency. The main object of research is the processes of discretisation and restoration of analogue signals in hybrid analogue-digital systems. The theoretical basis of the study is the analysis of the above-described architecture of the tracking-parallel analogue-digital converter. A structural-functional approach is used to decompose the proposed device into basic functional units: a tracking loop, a subtraction unit, a parallel quantiser (Flash Sub-ADC) and a digital summing unit. To analyse the dynamic characteristics and evaluate the conversion errors, a discrete mathematical model of the tracking-parallel analogue-to-digital converter operation in the time domain was developed, which provides mathematical modelling of dynamic processes.

The operation of a classic tracking circuit is described by a recursive relationship:

$$U_{TR}[n] = U_{TR}[n-1] + \Delta_{LSB} \cdot sgn(U_{in}[n] - U_{TR}[n-1]), \quad (1)$$

where $U_{TR}[n]$ – output voltage of the digital-to-analogue converter of the tracking circuit at the n-th clock cycle; $U_{in}[n]$ – input signal; Δ_{LSB} – quantisation step.

The dynamic error (inconsistency error) that occurs when the input signal exceeds the tracking speed is defined as:

$$\varepsilon[n] = U_{in}[n] - U_{TR}[n]. \quad (2)$$

In the proposed model of a tracking-parallel analogue-to-digital converter, this error is not discarded but scaled with the amplification factor G and quantised by a parallel analogue-to-digital converter. The conversion function of the parallel block is described as:

$$D_{FL}[n] = Q_{Flash}(G \cdot \varepsilon[n]), \quad (3)$$

where Q_{Flash} – quantisation function of a parallel analogue-to-digital converter with a bit width of K.

The resulting output code of the system $D_{OUT}[n]$ is formed as the sum of the codes of the main and corrective channels:

$$D_{OUT}[n] = D_{TR}[n] + \frac{1}{G} \cdot D_{FL}[n]. \quad (4)$$

The criterion for the absence of slope overload in the model is the condition under which the amplitude of the differential signal $\varepsilon[n]$ does not exceed the input dynamic range of the parallel analogue-to-digital converter. To formalise the quantisation process, the following basic relationships are used in the study. The quantisation step (LSB) is determined by the dynamic range of the reference voltage and the bit width:

$$\Delta = \frac{V_{ref}}{2^N}. \quad (5)$$

The ideal quantisation error, which determines the theoretical limit of accuracy, is half the quantisation step:

$$\varepsilon_q = \frac{\Delta}{2}. \quad (6)$$

The output digital code is formed as a weighted sum of digits:

$$D = \sum_{i=0}^{2^N-1} D_i \cdot 2^i. \quad (7)$$

A key aspect of the study is the analysis of the behavioural model of the tracking circuit. Its response to input in continuous time is described by the differential equation of capacitance charge (integrator) or an equivalent RC circuit model:

$$\frac{dV_c(t)}{dt} = \frac{V_{in}(t) - V_c(t)}{RC}. \quad (8)$$

The solution to this equation for the voltage surge is as follows:

$$dV_c(t) = V_{in}\,1 - e^{-t/(RC)}. \quad (9)$$

A classic tracking analogue-to-digital converter changes the output code by only 1 LSB per clock

cycle. This imposes a strict limitation on the maximum input signal change rate (slew rate). The condition for error-free tracking for a classic circuit is:

$$\left|\frac{dV_{in}}{dt}\right| \le \frac{\Delta}{T_s}. \quad (10)$$

The tracking analogue-to-digital converter changes the code by 1 LSB per clock cycle. The flash channel compensates for the remainder, but not for the infinite derivative. Therefore, a maximum signal speed was introduced:

$$\left|\frac{du_{in}}{dt}\right|_{max}. \quad (11)$$

Without a Flash converter, the condition is classic:

$$\left|\frac{du_{in}}{dt}\right| \le \frac{\Delta_{tr}}{T_s}. \quad (12)$$

In the proposed tracking-parallel analogue-to-digital converter, an additional Flash channel is introduced, which is capable of instantly compensating for the residual (tracking error). If the Flash analogue-to-digital converter has a resolution of *Nfl*, it covers the range of $2^{N_{fl}}$ steps of the tracking analogue-to-digital converter.

Accordingly, the new condition for the maximum signal rise rate takes the form:

$$\left|\frac{du_{in}}{dt}\right| \le \frac{\Delta_{tr}}{T_s} 1 + 2^{N_{fl}} - 1 = \frac{2^{N_{fl}}\Delta_{tr}}{T_s}. \quad (13)$$

The settling time is also a critical parameter. Since the error signal is formed and measured within a single clock cycle, the OP transition process must be completed with the specified accuracy during the active phase of the clock signal. Assuming a clock pulse duty cycle of 50% (meander), the boundary condition for the settling time is defined as half the sampling period.

This leads to an analytical expression for the maximum speed of a hybrid system:

$$S_{max}\left|\frac{du_{in}}{dt}\right|_{max} = \frac{2^{N_{fl}}\Delta_{tr}}{T_s}. \quad (14)$$

Comparing this with the maximum speed of a classic Tracking-ADC:

$$S_{max}^{Tracking} = \frac{\Delta_{tr}}{T_s}. \quad (15)$$

The performance gain factor was obtained:

$$S_{max} = 2^{N_{fl}} S_{max}^{Tracking}. \quad (16)$$

Speed increase multiplier = $2^{N_{fl}}$. To evaluate the metrological characteristics of the system, a total error model is used, which includes quantisation error, zero offset, gain error and noise:

$$\varepsilon_{total} = \sqrt{\varepsilon_q^2 + \varepsilon_{offset}^2 + \varepsilon_{gain}^2 + \varepsilon_{noise}^2}. \quad (17)$$

Integral (INL) and differential (DNL) nonlinearities are calculated using standard formulas:

$$INL = max_i \left|\frac{V_{real}(i) - V_{ideal}(i)}{\Delta}\right|, DNL(i) = \frac{V_{i+1} - V_i}{\Delta} - 1. \quad (18)$$

The resulting signal in the tracking-parallel architecture is formed as the sum of a rough estimate and a refined estimate, scaled by a coefficient:

$$X = Q_1(V_{in}) + K \cdot Q_2 V_{in} - V_{DAC}. \quad (19)$$

Error after correction:

$$\varepsilon_{comb} \frac{V_{ref}}{2^{N_1+N_2+1}}. \quad (20)$$

The dynamic error of the system until compensation is achieved is:

$$\varepsilon(n) = u_{in}(n) - u_{DAC}(n) - k_{fl}(n)\Delta_{fl}. \quad (21)$$

Since Flash operates in an error loop, it accurately restores the discrepancy value if it is within its dynamic range:

$$|\varepsilon(n)| \le \frac{\Delta_{fl}}{2}. \quad (22)$$

To verify the advantages of the developed architecture, a comparison with analytical models of classical converters is performed. Flash analogue-to-digital converters are characterised by maximum speed but have high error due to the complexity of matching a large number of comparators:

$$\varepsilon_{total}^{Flash} = \frac{V_{ref}}{2^{N+1}},\ f_s \approx \frac{1}{T_c}. \quad (23)$$

The SAR analogue-to-digital converter has a limited sampling frequency due to the need for *N* cycles per conversion:

$$\varepsilon_{total}^{SAR} = \frac{V_{ref}}{2^{N+1}} + \varepsilon_{logic}, T_s = N \cdot T_{clk}. \quad (24)$$

Sigma-Delta (ΣΔ) analogue-to-digital converters provide high accuracy through oversampling (*OSR*), but have the lowest speed:

$$X_{out} = {}^{T}_{0}(V_{in} - V_{DAC})dt, \varepsilon_q^{\Sigma\Delta} \approx \frac{\Delta}{\sqrt{OSR}}, \quad (25)$$

where *OSR* – upsampling factor.

The proposed tracking-parallel model combines the high instantaneous speed of the Flash method (within the error window) with the accuracy and simplicity of the tracking method. The simulation modelling methodology involved verification of analytical calculations by means of computer modelling in the MATLAB/Simulink environment. For this purpose, a behavioural model of the converter was created, which incorporates the discreteness in time and level, the limited rate of rise of the output voltage of the operational amplifier, as well as signal propagation delays in logic elements and the settling time of the digital-to-analogue converter.

A harmonic signal ($U[t] = A \cdot sin(2\pi ft)$) was used as a test stimulus to determine the effective number of bits (ENOB) and signal-to-noise ratio (SNR) in the frequency domain, and a pulse signal (Heavisine function) was used to study transient processes and the system's response to instantaneous voltage jumps. The comparative evaluation method consisted of determining the efficiency of the proposed architecture by comparative analysis with traditional architectures (Flash ADC and SAR ADC) according to the following criteria: hardware complexity, slew rate, and power consumption. Hardware complexity (H) was evaluated by the number of comparators (N_{comp}) as the most energy-intensive elements of the circuit. For an N-bit converter:

Parallel analogue-to-digital converter (Flash):

$$H \approx 2^N. \quad (26)$$

Tracking parallel analogue-to-digital converter:

$$H \approx 1 + 2^K, \quad (27)$$

where $K \ll N$ bit depth of the parallel sub-analogue-to-digital converter.

Slew Rate is the maximum rate of change of the input signal that an analogue-to-digital converter can reproduce without distortion. Power consumption – the qualitative assessment was based on the number of active analogue components in the conversion cycle. The Waldon formula, adapted for hybrid structures, was used to calculate the Figure of Merit (FoM). A combined approach was used to ensure the reliability of the results. An analytical calculation was performed: the slew rate limit, theoretical dynamic range, and SNR ratio were determined based on the above mathematical models for ideal conditions. Simulation modelling was also performed: ENOB and system behaviour during transient processes were obtained by modelling in the MATLAB environment. The model incorporates the actual delays of comparators ($\tau_{comp} = 0.1 \cdot T_{clk}$) and the limited slew rate of the operational amplifier. The calculations were performed for a hypothetical implementation according to 180 nm process technology standards, $V_{ref} = 1.8$B, $f_{clk} = 100$ MHz.

A comprehensive indicator that incorporates the balance between speed, accuracy and complexity was chosen as the criterion for efficiency. For comparative analysis, a list of analogous architectures that are dominant in their respective niches was determined in advance. Flash analogue-to-digital converter – as a benchmark for speed (but with high complexity 2^N). SAR analogue-to-digital converter – as a benchmark for energy efficiency (but with limited speed $T_s \cdot N$). $\Sigma\Delta$ analogue-to-digital converter – as a benchmark for accuracy (but with low speed due to oversampling). The comparison is based on the following criteria: maximum sampling frequency (f_s), ENOB, hardware complexity (number of comparators) and relative power consumption. To confirm the proposed recursive relationships and evaluate the effectiveness of overload elimination, a numerical calculation was performed for a specific set of parameters characteristic of modern embedded systems. Model parameters: total bit width of the analogue-to-digital converter: $N = 12$ bits, full-scale voltage: $V_{FS} = 2.0$V, clock frequency: $f_{clk} = 100$ MHz ($period T_s = 10$ ns), bit width of the auxiliary Flash block: $N_{fl} = 4$ bits. The selected mode of 12 bits at 100 MHz is indicative of modern electric motor control systems and telecommunications interfaces, where classic SAR ADCs no longer provide the required performance, and Flash ADCs are excessively expensive. A voltage of 2.0 V is a typical full scale for analogue interfaces of low-voltage microcontrollers. The 4-bit Flash block resolution was chosen as the sweet spot, increasing the response speed by 16 times while using only 15 additional comparators, which has a negligible impact on the chip area.

RESULTS AND DISCUSSION

For the correct positioning of the proposed method, it is necessary to consider the basic principles of existing architectures and identify their strengths and weaknesses. Parallel analogue-to-digital converters (Flash ADCs) and direct conversion architecture (Flash) are based on simultaneous comparison of the input signal with a set of reference voltages. They contain a resistive divider and an array of comparators. The principle of operation is as follows: the input signal is fed in parallel to 2^{N-1} comparators. The reference inputs of the comparators are connected to the corresponding nodes of the voltage divider. The result of the comparison forms a thermometric code, which is then converted into a binary code. The advantages of this principle are that it provides the fastest possible performance, since the conversion is instantaneous (in one clock cycle). The absence of feedback loops renders this architecture suitable for ultra-fast applications. However, the main drawback is hardware redundancy. A 10-bit analogue-to-digital converter requires 1,023 comparators, and a 12-bit converter requires 4,095. This results in significant power consumption, large chip area, and high input capacitance, which complicates the operation of the input buffer.

Tracking ADCs belong to the class of feedback systems and are based on a reversible counter. The principle of operation is as follows: The system continuously "tracks" the input signal. A comparator compares the input voltage with the output of the feedback digital-to-analogue converter. If the input signal is greater, the counter increments; if it is smaller, it decrements. The advantages of this principle are its simplicity of implementation (only one comparator is required), the absence of complex sampling and storage circuits, and high energy efficiency when working with slow-changing signals. However, the disadvantages are that the response speed is limited. The maximum speed of change

of the output code is 1 LSB per clock cycle. During the processing of high-frequency or pulse signals, a slope overload error occurs when the output code does not have time to catch up with the input voltage.

SAR uses a binary search (dichotomy) algorithm. It is the energy efficiency standard for medium speeds, but requires *N* cycles to obtain one reading, which limits its maximum frequency. Sigma-delta is based on resampling and noise shaping. It provides ultra-high accuracy (24 bits and above), but has high latency and limited bandwidth. However, there is a problem of versatility: none of the classic architectures is optimal for all cases. Flash is too expensive and hot for high accuracy, Tracking is too slow for dynamics, and SAR is a compromise but does not reach Flash speeds. Hybrid solutions (Pipeline, Two-Step) attempt to combine the advantages, but often inherit the disadvantages (calibration complexity, latency). The tracking-parallel architecture proposed in this work is an attempt to solve the problem of versatility by dynamically redistributing the load between the "slow" accurate channel and the "fast" coarse channel. The presence of negative feedback through a digital-to-analogue converter ensures high system stability. The architecture also demonstrates increased noise immunity: the tracking loop acts as a noise integrator, while the parallel channel compensates for random impulse disturbances, preventing tracking failure.

The practical implementation of the device requires precise matching of the operational amplifier gain to the dynamic range of the parallel analogue-to-digital converter. It also requires sufficient speed of the operational amplifier, which must ensure that the output voltage is established in less than half a clock cycle. In addition, initial calibration is necessary to eliminate zero offset between the two conversion channels. Based on formula (17) of the total error of the converter ε_{total}, the contribution of individual components was evaluated.

Quantisation error ε_q: for a 12-bit system, LSB is:

$$\Delta = \frac{2.0}{2^{12}} \approx 488 \text{ mV}. \quad (28)$$

Theoretical root mean square quantisation error:

$$\varepsilon_q = \frac{\Delta}{\sqrt{12}} \approx 141 \text{ mV}. \quad (29)$$

Offset error ε_{offset}: Incorporating the use of zero auto-correction technology in the operational amplifier and comparators, the residual offset voltage at the input is estimated at 0.2 LSB:

$$\varepsilon_{offset} = 0.2 \cdot \Delta \approx 98 \text{ mV}. \quad (30)$$

Transmission coefficient error ε_{gain}: determined by the accuracy of the scale resistor and the OP gain coefficient. When using precision thin-film resistors (with an accuracy of 0.1%) and calibration, the residual gain error is approximately 0.15 LSB:

$$\varepsilon_{gain} = 0.15 \cdot \Delta \approx 73 \text{ mV}. \quad (31)$$

Noise component ε_{noise}: includes thermal noise of resistors and input noise of the OP. For a passband of 100 MHz, the integral noise is estimated as:

$$\varepsilon_{noise} \approx 120 \text{ mV}. \quad (32)$$

Final accuracy:

$$\varepsilon_{total} = \sqrt{141^2 + 98^2 + 73^2 + 120^2} \approx 220 \text{ mV}. \quad (33)$$

This value is less than half of the LSB (244 μV), confirming the possibility of achieving the claimed 12-bit accuracy. The maximum signal recovery error recorded during modelling was 235 μV, which is consistent with the calculated value.

The maximum speed of a classic tracking analogue-to-digital converter, under condition $|dV/dt| \leqslant \Delta/T_s$:

$$SR_{track} = \frac{488 \cdot 10^{-6}}{10 \cdot 10^{-9}} = 48.8 \frac{kV}{c} = 0.0488 \frac{V}{mks}. \quad (34)$$

For a sinusoidal signal with amplitude A = 1V ($V_{in} = A\sin(2\pi ft)$), the maximum slew rate is $2\pi fA$. Therefore, the maximum frequency without overload is:

$$f_{max\ track} = \frac{SR_{track}}{2\pi A} \approx \frac{48{,}800}{6.28} \approx 7.77 \text{ kHz}. \quad (35)$$

This result confirms that the classical scheme is unsuitable for processing audio or video signals even at high clock frequencies. The maximum speed of a tracking-parallel analogue-to-digital converter: Thanks to the introduction of a 4-bit Flash ADC, the system can compensate for an error of up to $2^4 = 16$ LSB per clock cycle:

$$SR_{hybrid} = 16 \cdot SR_{track} = 16 \cdot 0.0488 \approx 0.78 \frac{v}{mks}. \quad (36)$$

Corresponding signal cut-off frequency:

$$f_{max\ hybrid} \approx \frac{0.78 \cdot 10^6}{6.28} \approx 124 \text{ kHz}. \quad (37)$$

Thus, theoretical calculations show a 16-fold increase in the permissible input signal frequency, which fully corresponds to the derived acceleration coefficient ($2^{N_{fl}}$) formula. When a 120 kHz signal was applied to the model input, the system maintained stable tracking, while the classic Tracking ADC entered overload mode at 8 kHz. During testing in the operating frequency range, the maximum recorded signal recovery error did not exceed ±0.5 LSB (which is ≈ 0.24 mV), confirming the effectiveness of dynamic component compensation by a parallel block. Although increasing the bit width of the Flash block (N_{fl}) theoretically can be used for exponential performance gains, practical implementation is hampered by physical limitations that must be considered during design.

Exponential growth in complexity: Flash parts at $N_{fl} = 4$ require 15 comparators, which is acceptable. At $N_{fl} = 6$, there are already 63, and at $N_{fl} = 8$, there are 255. This negates the advantage of a small crystal area and increases the parasitic capacitance at the Flash block input. Requirements for the operational amplifier (Slew Rate Bottleneck): as N_{fl} increases, the amplitude of the residual signal that must be amplified by the analogue path (OP) increases. If $N_{fl} = 6$, then the OP must be capable of producing a voltage jump corresponding to 64 LSB in time $\frac{T_s}{2}$. This means that the requirements for the rise time of the OP output voltage (SR_{OP}) increase proportionally to $2^{N_{fl}}$. At a certain point (usually when $N_{fl} > 5$-6), the power consumption of the ultra-fast OP begins to exceed the benefits of using a hybrid circuit.

Optimal operating point: analysis showed that the optimal range for N_{fl} is 3-5 bits. In this corridor, a significant (8-32 times) increase in dynamic stability is achieved while maintaining the compactness of the circuit and moderate requirements for analogue components. To confirm the effectiveness of the proposed hybrid solution, a comparative analysis of its key characteristics with basic architectures was conducted. Table 1 below illustrates the place of the tracking-parallel analogue-to-digital converter among existing technologies.

Table 1. Comparison of quality indicators of the main architectures of analogue-to-digital converters

Characteristic	Flash ADC	SAR ADC	ΣΔ (Sigma-Delta)	Tracking-Parallel ADC (proposed)
Speed	High (1 cycle)	Average (*N* cycles)	Low	High (signal adaptive)
Bit width	Low / Average (6-10 bit)	Average / High (8-16 bit)	High (16-24+ bit)	Average / High (bit width sum)
Linearity	Determined by resistors	Depends on the digital-analogue converter	Variable	High (due to feedback)
Noise	High (wide band)	Average	Low (in signal band)	Low (filtering properties of the circuit)
Hardware complexity	High (2*N* components)	Low	Complex digitally	Average (2 components, where $K \ll N$)
Energy consumption	High (up to 520 W)	Low (10 – 100 mW)	Average (50 – 500 mW)	Average (savings on the number of comparators), 310 times lower than Flash
Sphere of use	Oscilloscopes, Radars	Data collection system, Sensors	Audio, metrology	Video, Fast Control Loops, Broadband Sensors

Source: compiled by the authors

Difference from a parallel analogue-to-digital converter (Flash): the main advantage of the proposed solution is a significant reduction in hardware complexity. While a 10-bit Flash analogue-to-digital converter requires 1,023 comparators, a tracking-parallel analogue-to-digital converter of the same bit width (e.g., 6 bits Tracking + 4 bits Flash) requires only about 16-20 comparators. This significantly reduces the chip area and power consumption while maintaining a high response speed to signal changes. This is consistent with the principles of systematic mixed-signal design outlined by M. Fakhfakh *et al.* (2013), emphasising the need to minimise active chip area to reduce cost and increase reliability.

The difference from the SAR analogue-to-digital converter is that it spends a fixed amount of time (several cycles) on each count, which limits its maximum sampling frequency. A tracking-parallel analogue-to-digital converter in tracking mode updates the output code on each clock cycle, providing virtually continuous signal tracking with minimal latency, which is critical for real-time automatic control systems. The difference from the ΣΔ analogue-to-digital converter is the absence of signal processing latency and bandwidth limitations inherent in the ΣΔ architecture. While ΣΔ analogue-to-digital converters achieve high accuracy through significant oversampling and the use of complex digital decimation filters, which inevitably introduce group delay and make them unsuitable for processing fast transient processes, a follow-up parallel analogue-to-digital converter operates with instantaneous input signal values. Therefore, the proposed architecture can be used in broadband applications (video signals, radars) and fast closed-loop control systems, where phase delays characteristic of ΣΔ modulators can lead to loss of system stability. Based on the analysis and mathematical modelling, a comprehensive comparison table of the characteristics of the main types of analogue-to-digital converters and the proposed hybrid solution was created (Table 2).

Table 2. Comparison of quantitative indicators of the main architectures of analogue-to-digital converters

Parameter	Flash ADC	SAR ADC	ΣΔ (Sigma-Delta) ADC	Tracking-Parallel ADC (proposed)
Typical bit width range (N)	48 bit	816 bit	1,624 bit	1,014 bit
Maximum sampling rate	120 GHz	150 MHz	15 MHz	100 – 150 MHz
Quantisation step Δ	$2NV_{ref}/2^N$	same	same (OSR effectively decreases)	reduced due to clarification
DNL / INL	0, 51, 0 LSB	0,250,5 LSB	<0.1 LSB	0, 10, 25 LSB
SNR (for 10 bit)	5,056 dB	5,860 dB	80,100 dB	6,268 dB
ENOB (effective bits)	67	911	1,521	1,012
Required number of comparators	2^{N-1}	1	1	432 (depending on the clarifying block)

Source: compiled by the authors

When analysing performance, Flash analogue-to-digital converters remain the absolute leaders thanks to the complete parallelism of the conversion process. In contrast, the SAR analogue-to-digital converter is limited by the need to perform N comparison cycles to obtain a single reading, and the ΣΔ architecture, despite its high accuracy, has a slow output due to the need for digital filtering and decimation. In this context, the follow-up parallel analogue-to-digital converter wins in terms of speed compared to SAR and ΣΔ, since the result is refined by a fast parallel block in the same clock cycle (or with minimal delay) as the main circuit. In terms of accuracy (ENOB), Flash architecture often suffers from the offset of a large number of comparators, which reduces the effective bit width. The highest ENOB is demonstrated by the ΣΔ analogue-to-digital converter due to noise formation. A successive approximation analogue-to-digital converter increases accuracy through double conversion: coarse tracking and precise measurement of the remainder, supporting ENOB at 1,012 bits even at high frequencies.

An assessment of energy consumption and hardware complexity shows that Flash analogue-to-digital converters scale exponentially, remaining the most expensive and "hottest" option, requiring 1,013 comparators for 10 bits. SAR is the most economical, requiring only one comparator, but it is inferior in speed. The hybrid (serial-parallel) option demonstrates moderate consumption, and the number of comparators is determined by the formula $N_{comp}^{Hybrid} \approx 2^{N_{fl}} - 1$, where N_{fl} is the bit width of the parallel refinement block. For a typical implementation, this is 1,531 comparators, which is dozens of times less than a full Flash analogue of the same bit width. In summary, it is possible to state that the Flash analogue-to-digital converter is the fastest, but energy-intensive and low-bit, while SAR is a compromise between accuracy and consumption, being limited by speed, and ΣΔ is the most accurate, but the slowest. The follow-up parallel analogue-to-digital converter provides an optimal balance, especially for the 1,014-bit range and speeds up to 500 MS/s. It combines adaptability to rapid signal changes (thanks to the Flash insert) with the accuracy of a closed-loop control system.

Analysis of the results obtained through the prism of fundamental works can identify critical engineering challenges in implementing the proposed architecture. The proposed hybrid architecture is characterised by several unique properties that distinguish it from its counterparts. The combination of tracking and parallel methods provides the system with dual properties. In quasi-stationary mode, when the signal changes slowly, it functions as a high-precision tracking circuit with minimal error. During fast transients, the architecture adapts instantly: the parallel channel digitises the dynamic difference, effectively expanding the equivalent bandwidth. Thanks to this adaptability, the system is capable of correctly processing signals with variable spectral density. This behaviour is consistent with the concept of "smart" data converters described by A.H.M. Roermund *et al.* (2010), where adaptability to input signal characteristics is considered a key direction for improving the energy efficiency of modern microcircuits. A key engineering advantage is the reduction of quantisation error in dynamic mode. In contrast to the traditional "sawtooth" overload characteristic of delta modulators, the output signal accurately replicates the shape of the input signal by adding an error code. This contributes to an increase in the linearity of the output characteristic, since the residual error does not accumulate but is corrected at each conversion cycle. The parallel analogue-to-digital converter acts as a dynamic buffer. A classic tracking analogue-to-digital converter is limited to a change of only 1 LSB per clock cycle. As noted by the authors in their reference book, U. Tietze *et al.* (2008), this is the main factor that makes it impossible to use such analogue-to-digital converters for processing broadband signals. Also, in the fundamental work by B. Razavi (1995), it is noted that two-step architectures can circumvent the speed limitations of sequential methods, but usually require complex sampling-storage circuits. However, the proposed architecture can correctly reproduce an amplitude jump to 2^{K-1} LSB in one clock cycle (where K – Flash section bit width). This significantly

increases the slew rate without the need to increase the clock frequency.

In classic Flash analogue-to-digital converters, the input signal is fed to hundreds or thousands of parallel comparators, creating a huge capacitive load on the signal source. The fundamental work by P. Horowitz & W. Hill (2015) emphasises that such input capacitance requires powerful and energy-intensive input buffers, which often negate the advantages of high speed. In the proposed architecture, the input signal is loaded only onto one comparator (tracking circuit) and the input of the operational amplifier, which greatly simplifies the requirements for the signal source. As described in detail in R. van de Plassche (2003), reducing input capacitance is critical for high-frequency applications as it can expand bandwidth without increasing the power consumption of the driver. T.C. Carusone *et al*. (2011) investigated the fundamental limitations of the speed of closed analogue circuits. The study concluded that the accuracy of the output voltage setting depends exponentially on the product of the bandwidth and the settling time, and the linearity is determined by the depth of feedback. Comparing these conclusions with the simulation results, it can be argued that for the correct operation of a tracking-parallel ADC, it is critical to ensure that the slew rate of the operational amplifier exceeds the maximum slope of the error signal. Failure to meet this condition, as predicted by the researchers, leads to dynamic nonlinear distortions, which were observed in simulations at frequencies above 125 kHz.

Scientist F. Maloberti (2007) conducted a detailed study of the conversion stages in conveyor and multistage ADCs. The study concluded that the amplifier settling time must be strictly less than half the clock frequency to avoid charge transfer errors between stages. In the context of the study, this means that the operational amplifier that forms the residual signal must have a settling time of no more than 5 ns (for f_{clk} = 100 MHz). This confirms that the OP is the "bottleneck" that limits the maximum sampling frequency of a hybrid ADC compared to a Flash converter. M. Fakhfakh *et al*. (2013) studied the effect of technological parameter variation on the characteristics of mixed circuits. The study determined that variation in multi-path architectures is the dominant source of nonlinear distortions that cannot be eliminated by circuit design methods alone. A comparison with the proposed architecture shows that the discrepancy in the transfer coefficient between the OP and the digital weights of the Flash ADC leads to DNL errors at the range switching boundaries. This correlates with the monograph by M.J. Pelgrom (2010), proving that passive matching becomes geometrically inefficient for accuracies above 10 bits. Therefore, the proposed solution requires the implementation of digital calibration algorithms similar to those described in the paper to achieve the claimed 12-bit accuracy.

R.J. Baker (2008) studied the mechanisms of noise generation in mixed signals, in particular the "backlash" effect from dynamic comparators. The study concluded that this noise can significantly distort the input signal if the source has high impedance. In contrast to the author's conclusions for Flash ADCs, the study observed less sensitivity to this effect. This is attributed to the fact that the tracking circuit acts as a low-impedance driver and filter, confirming the thesis of increased noise immunity of the hybrid circuit. D.-R. Oh *et al*. (2022) investigated a 7-bit two-step Flash ADC that uses a sampling-storage sharing (S/H sharing) technique to reduce chip area. The study concluded that this architecture can achieve a sampling rate of 2.5 GHz with low power consumption. Compared to the study, the tracking-parallel architecture also reduces the number of comparators, but the advantage is determined by the absence of a strict need for complex clocking of the S/H device for the tracking circuit, since it operates in continuous tracking mode, which can provide lower latency for certain classes of signals.

K.E. Lozada *et al*. (2024) analysed hybrid SAR-based architectures, specifically SAR-Flash and SAR-Pipeline, to improve energy efficiency. Their findings indicate that using SAR for coarse quantisation significantly reduces energy consumption compared to full Flash circuits. Compared to these results, the proposed tracking-parallel method offers an alternative compromise: instead of using iterative (and therefore slower) SAR for accurate approximation, a fast Flash block is used for instantaneous error correction. This makes the architecture potentially faster for real-time signal tracking tasks, although possibly less energy-efficient than SAR. F. Shahbazi & H. Shamsi (2025) presented a Level-Crossing ADC with a 1-bit DAC and a continuous-time comparator. The authors achieved ultra-low power consumption due to the asynchronous nature of the operation. However, their approach has limitations in terms of accuracy and linearity due to the use of 1-bit feedback. The proposed architecture, in contrast, uses a multi-bit tracking circuit and a multi-bit Flash corrector, which provides significantly higher linearity (10-12 bits) and better response to fast signal changes, while maintaining the adaptive power consumption advantages inherent in feedback systems.

H. Tang *et al*. (2024) proposed a hybrid LC-SAR that combines a level crossing detector (LC) with SAR logic for Internet of Things (IoT) applications. They achieved high energy efficiency (0.494.34 μW), but the bandwidth is limited to 20 kHz. In comparison, the proposed tracking-parallel ADC targets a much wider frequency range (hundreds of kHz to MHz), as the use of a Flash section for residual processing eliminates the speed bottleneck characteristic of sequential algorithms. M. Timmermans *et al*. (2024) investigated a 64-dB SNDR Continuous-Time Level Crossing ADC with dynamic self-offset comparators. They conclude that this technique achieves record energy efficiency for sparse signals. Compared to the research results, the proposed approach also exploits the idea of adaptability (the

Flash section is active only when there is a significant error), which can reach the energy efficiency of circuits, but with more deterministic time behaviour due to clocking, which simplifies digital processing. S.A. Zahrai & M. Onabajo (2018) highlighted how individual substructures affect energy consumption and performance, in particular, considering time-interleaved (TI) and sub-ranging architectures to achieve high sampling rates with low consumption. The study provided an example of a hybrid ADC implementation with a frequency of ~1 GS/s, where the first stage is a flash ADC and the second stage is four TI SAR-like blocks, and showed actual chip measurements confirming low power consumption at medium bit depth (~6-8 bits) and high speed.

In their review, S. Xiao *et al*. (2025) emphasised the need to create specialised ADCs for in-memory computing (CIM) systems, where a balance between area and accuracy is important. The proposed design fits this trend, as the absence of bulky capacitor arrays (characteristic of SAR) and a large number of comparators (Flash) provides compact solutions suitable for integration into complex computing arrays. K. Krishna & N. Nambath (2024) reviewed high-speed dynamic comparators, highlighting their role in the energy consumption of Flash ADCs. Since the proposed circuit uses only a low-bit-width (3-4 bits) Flash subsystem, the number of such energy-intensive elements is minimised, solving the problem and achieving a better FoM compared to traditional solutions. The results of the analysis confirmed that the track-and-parallel architecture is an effective hybrid solution that fills the niche between simple but slow track-and-parallel analogue-to-digital converters and fast but expensive Flash analogue-to-digital converters. It offers an optimal balance of parameters for a wide class of devices where both dynamic accuracy and moderate power consumption are relevant.

The study further developed the theory of designing hybrid analogue-to-digital converters. For the first time, the architecture in which a parallel analogue-to-digital converter is used not for traditional result refinement (as in sub-ranging schemes), but as a link of instantaneous negative feedback for error, has been studied in detail and mathematically substantiated. The study proved that this approach can transform main disadvantage of tracking systems – inertia – into a controllable parameter that is effectively compensated by a low-bit parallel block. This can be used for the creation of a new class of analogue-to-digital converters that combine high equivalent speed with minimal chip area and adaptive power consumption.

CONCLUSIONS

The paper presents a comprehensive study and mathematical modelling of a new architecture for a tracking-parallel analogue-to-digital converter. The simulation results confirmed that the proposed hybrid approach effectively solves the problem of the limited performance of classical tracking systems. In particular, the study determined that the integration of a K-bit parallel sub-converter into the error loop increases the maximum input signal rise rate by 2^K times. A numerical experiment for a 12-bit model with a 4-bit Flash module at a clock frequency of 100 MHz demonstrated an expansion of the operating frequency band from 7.77 kHz (for the classical circuit) to 124.2 kHz without the occurrence of slope overload distortions. At the same time, the dynamic signal recovery error across the entire range did not exceed ±0.5 LSB. A comparative analysis showed that the developed architecture provides a significant advantage in terms of hardware complexity. To implement 12-bit conversion, the proposed circuit requires fewer than 35 comparators, which is a 99% reduction in hardware costs compared to a classic Flash ADC (4,095 comparators). This provides high equivalent performance with significantly less chip area and power consumption than fully parallel analogues, and with lower latency than SAR architectures. The scientific novelty of the work lies in establishing and confirming the analytical relationship between the bit width of the auxiliary parallel channel and the dynamic range expansion factor of the tracking system. The practical value of the results is determined by the creation of a scalable solution for precision control and telemetry systems that can process broadband signals with an accuracy of 1,014 bits without the need for energy-intensive ultra-fast ADCs. Further work will focus on the hardware implementation of the device in modern nanometre CMOS technologies (2,865 nm) with the development of digital background calibration algorithms to compensate for channel mismatches. It is also planned to investigate methods of dynamic power management of individual blocks to minimise energy consumption in IoT applications.

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Анотація. В умовах стрімкого розвитку цифрових систем обробки сигналів актуальним стає завдання створення нових архітектур аналого-цифрових перетворювачів, здатних забезпечити високу динамічну точність без надмірного нарощування кількості компонентів. Метою роботи було підвищення динамічної точності та швидкодії процесу аналого-цифрового перетворення шляхом розробки та дослідження удосконаленої слідкувально-паралельної архітектури. Для досягнення поставлених завдань застосовано методи теорії автоматичного керування, схемотехнічного аналізу імпульсних пристроїв та математичного моделювання похибок квантування. У статті детально розглянуто принцип дії запропонованого пристрою, який базується на синергії інерційного слідкувального контуру та швидкодіючого паралельного перетворювача залишку. Доведено, що введення ланки вимірювання динамічної помилки дозволяє компенсувати відставання вихідного коду від вхідного сигналу, характерне для традиційних слідкувальних систем, і тим самим усунути спотворення внаслідок перевантаження за нахилом. Аналітично обґрунтовано залежність розширення динамічного діапазону вхідного сигналу від розрядності паралельного блоку, що дає змогу гнучко адаптувати систему під вимоги конкретного застосування. Результати порівняльного аналізу свідчать про те, що запропонована структура забезпечує суттєвий виграш в апаратній складності, дозволяючи реалізувати високу роздільну здатність із використанням на порядок меншої кількості прецизійних компараторів порівняно з аналогами. Також визначено критичні вимоги до швидкодії операційного підсилювача та цифро-аналогового перетворювача у колі зворотного зв'язку для забезпечення стабільної роботи у всьому частотному діапазоні. Практична цінність дослідження полягає в розробці рекомендацій для проєктування конкурентоспроможних мікросхем, орієнтованих на використання в портативних пристроях, медичній апаратурі та системах промислової автоматики

Ключові слова: гібридна архітектура; перевантаження за нахилом; компенсація динамічної похибки; сигнал залишку; швидкість наростання сигналу; апаратна ефективність; високоточність